

REPLACEMENT CLAIMS

- Sub C'*
1. (Twice Amended) A semiconductor device comprising:
- (a) a semiconductor substrate;
 - (b) an insulating film formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;
 - (c) a gate electrode formed on said semiconductor substrate;
 - (d) at least one sidewall covering said gate electrode therewith; and
 - (e) drain and source diffusion layers formed at a surface of said semiconductor substrate around said gate electrode,
- said at least one sidewall having a sidewall offset extending outwardly of said gate electrode along a surface of said semiconductor substrate in at least one of regions below which at least one of said drain and source diffusion layers are to be formed, said sidewall offset extending along a surface of a gate oxide film on which said gate electrode is formed,
- at least one of said drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset by an amount greater than a depth of said source and drain diffusion in a vertical direction.
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6. (Twice Amended) A semiconductor device comprising:

(a) a semiconductor substrate;

(b) an insulating film formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode formed on said semiconductor substrate;

(d) at least one sidewall covering said gate electrode therewith;

(e) drain and source diffusion layers formed at a surface of said semiconductor substrate around said gate electrode, said at least one sidewall having a sidewall offset extending outwardly of said gate electrode along a surface of said semiconductor substrate in at least one of regions below which at least one of said drain and source diffusion layers are formed, said sidewall offset extending along a surface of a gate oxide film on which said gate electrode is formed; and

(f) low-resistive wiring layers formed at surfaces of said drain and source diffusion layers, said low-resistive wiring layers being located outwardly beyond a peripheral edge of said sidewall offset in said at least one of said drain and source diffusion layers,

at least one of said drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset by an amount greater than a depth of said source and drain diffusion in a vertical direction.

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22. (Amended) The semiconductor device of Claim 6, wherein said sidewall

offset in said at least one of said drain and source diffusion layers extends only towards
one of said source and drain diffusion layers, the other of said at least one of said drain
and source diffusion layers having no sidewall offset.